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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/614,209	07/08/2003	Senthil Kumar Pandian	CSCO-031/7427	7332

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EXAMINER	
CHAN, SAI MING	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/614,209	PANDIAN, SENTHIL KUMAR	
	Examiner	Art Unit	
	Sai-Ming Chan	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/8/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statements (IDS) submitted on July 8, 2003 has been considered by the Examiner and made of record in the application file.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness

or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-5, 12-16, 23-27 and **34-38** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wei (U.S. Patent #6560196),** in view of **Radhakrishnan et al. (U.S. Patent Publication # 6049526).**

Consider **claims 1, 12, 23 and 34**, Wei clearly discloses and shows a method of sharing a line bandwidth on a communication path among a plurality of virtual circuits (fig. 4, column 9, lines 37-52 (VCs are grouped based on priority)) in an ATM Device (column 1, lines 64-67 (ATM)), said line bandwidth equaling a line rate (column 9, lines 5-7 (line rate)), wherein said plurality of virtual circuits comprise a plurality of VC-types (fig. 4; column 9, lines 24-34 (CBR & VBR), column 13, lines 16-19 (real time and non-real time), column 11, lines 7-9 (unspecific bit rate)), said method comprising:

accepting a configuration of said plurality of virtual circuits (fig. 4; column 9, lines

24-34 (CBR & VBR), column 13, lines 16-19 (real time and non-real time), column 11, lines 7-9 (unspecific bit rate));

receiving a plurality of cells (fig. 4, column 3, lines 56-58 (selecting cells for transmission)) on said plurality of virtual circuits (fig. 4; column 9, lines 24-34 (CBR & VBR), column 13, lines 16-19 (real time and non-real time), column 11, lines 7-9 (unspecific bit rate)); and

scheduling for transmission said plurality of cells on said communication path (fig. 4 (402), column 10, lines 37-52 (scheduling cells for transmission)) while enforcing a pre-specified priority with respect to said plurality of VC-types (fig. 4, column 9, lines 37-52 (VCs are grouped based on priority)) and while limiting bandwidth usage by each of said plurality of virtual circuits to a corresponding allocated bandwidth (column 9, lines 5-10 (based on the SCR on the VC)).

However, Wei does not specifically disclose a sum of allocated bandwidths of said plurality of virtual circuits exceeds said line rate.

In the same field of endeavor, Radhakrishnan et al. clearly show a sum of allocated bandwidths of said plurality of virtual circuits exceeds said line rate (column 13, lines 25-30 (exceeds the line rate)).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to demonstrate sharing a line bandwidth, as taught by Wei, and show allocated bandwidth exceeds line rate, as taught by Radhakrishnan, so that virtual circuits can be managed efficiently.

Consider **claim 2**, and **as applied to claim 1 above**,

claim 13, and **as applied to claim 12 above**,

claim 24, and **as applied to claim 23 above**,

claim 35, and **as applied to claim 34 above**,

Wei, as modified by Radhakrishnan et al., clearly discloses and shows a method, wherein said plurality of VC-types comprise constant bit rate (CBR) VC-type, variable bit rate-real time (VBR-RT) VC-type, variable bit rate non real time (VBR-nRT) VC-type (column 9, lines 24-34 (CBR & VBR), column 13, lines 16-19 (real time and non-real time)), wherein said pre-specified priority comprises highest to lowest priority for CBR VC-type, VBR-RT VC-type and VBR-nRT VC-type in that order (fig. 4; column 9, lines 24-34 (CBR & VBR), column 13, lines 16-19 (real time and non-real time)), wherein a first cell related to a lower priority VC-type is scheduled for transmission only if no cells of a higher priority VC-type are ready for transmission (fig. 4(408, 412), column 10, lines 53-56 (go to next highest priority)).

Consider **claim 3**, and **as applied to claim 2 above**,

claim 14, and **as applied to claim 13 above**,

claim 25, and **as applied to claim 24 above**,

claim 36, and **as applied to claim 35 above**,

Wei, as modified by Radhakrishnan et al., clearly discloses and shows a method, wherein said plurality of VC-types further comprises unspecified bit rate (UBR) VC-type (column 11, lines 7-9 (unspecific bit rate)), wherein UBR VC-type is given lower priority than said VBR-nRT VC-type (column 11, lines 7-9 (UBR has the lowest priority)).

Consider **claim 4**, and **as applied to claim 2 above**,

claim 15, and **as applied to claim 13 above**,

claim 26, and **as applied to claim 24 above**,

claim 37, and **as applied to claim 35 above**,

Wei, as modified by Radhakrishnan et al., clearly discloses and shows a method, wherein said scheduling comprises:

determining cell slots in which of each of said plurality of virtual circuits is a candidate for allocation according to a corresponding allocated bandwidth (fig. 4 (402), column 10, lines 37-52), wherein a first virtual circuit of a first VC-type (fig. 4 (404), column 10, lines 37-52) and a second virtual circuit of a second VC-type (fig. 4 (412), column 10, lines 37-52 (continues at 432)) are determined to be candidates for allocation in a first cell slot on said communication path, wherein said first VC-type is different from said second VC-type (column 10, lines 37-52 (CBR and next highest priority)); and

allocating said first cell slot to one of said first virtual circuit (fig. 4 (402), column 10, lines 37-52 (CBR)) and said second virtual circuit (fig. 4 (402), column 10, lines 37-

52 (next priority group)) having a higher priority (column 9, lines 24-34 (CBR & VBR)) if the virtual circuit with the higher priority has a cell ready for transmission (fig. 4 (410 and 422), column 10, lines 53-64).

Consider **claim 5**, and **as applied to claim 4 above**,

claim 16, and **as applied to claim 15 above**,

claim 27, and **as applied to claim 26 above**,

claim 38, and **as applied to claim 37 above**,

Wei, as modified by Radhakrishnan et al., clearly discloses and shows a method, wherein said scheduling further comprises allocating said first cell slot to one of said fast virtual circuit (fig. 4 (402), column 10, lines 37-52 (scheduling cells for transmission)) and said second virtual circuit having a lower priority (fig. 4 (412), column 10, lines 37-52 (continues at 432)) if the virtual circuit with the higher priority does not have a cell ready for transmission (fig. 4 (408, 412), column 10, lines 53-64) and if the virtual circuit with the lower priority has a cell ready for transmission (fig. 4 (412-422), column 10, lines 53-64).

Claims 6, 17, 28 and **39** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wei (U.S. Patent # 6560196)**, in view of **Radhakrishnan et al.**

(U.S. Patent Publication # 6049526), and in view of **Chen (U.S. Patent # 5533009).**

Consider **claim 6**, and **as applied to claim 5 above**,

claim 17, and **as applied to claim 16 above**,

claim 28, and **as applied to claim 27 above**,

claim 39, and **as applied to claim 38 above**,

Wei, as modified by Radhakrishnan et al., clearly discloses and shows a method as decribed.

However, Wei, as modified by Radhakrishnan et al., does not specifically disclose VC-credit counter.

In the same field of endeavor, Chen clearly shows scheduling further comprises:

maintaining a VC-credit counter associated with a fourth virtual circuit comprised in said plurality of virtual circuits (col. 2, lines 64-67, column 3, lines 1-4 (VCs)), wherein said VC-credit counter (fig. 5 (148 (I.sub.i), column 10, lines 50-55 (I.sub.i (cells that have not been output)) indicates a number of cells of backlog (column 10, lines 50-55 (I.sub.i (backlog)) for said fourth virtual circuit according to the corresponding allocated bandwidth (column 10, lines 50-55 (bandwidth management)), but limited by a maximum number (column 14, lines 24-26 (burst transmission rate)) specified by a VC-type of said fourth virtual circuit, wherein each cell slot on said communication path is allocated to said fourth virtual circuit only if said VC-credit counter is at least greater

than or equal to one (column 10, lines 63-66 (at least one cell)).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to demonstrate sharing a line bandwidth, as taught by Wei, and incorporate VC-credit counter, as taught by Chen, so that that virtual circuits can be managed efficiently.

Claims 7-9, 18-20, 29-32 and **40-42** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wei (U.S. Patent # 6560196),** in view of **Radhakrishnan et al. (U.S. Patent Publication # 6049526),** and in view of **Chen (U.S. Patent # 5533009),** and further in view of **Turner (U.S. Patent Publication #5179556).**

Consider **claim 7**, and **as applied to claim 6 above**,

claim 18, and **as applied to claim 17 above**,

claim 29, and **as applied to claim 28 above**,

claim 40, and **as applied to claim 39 above**,

Wei, as modified by Radhakrishnan and Chen, clearly discloses and shows a method as described.

However, Wei, as modified by Radhakrishnan and Chen, does not specifically disclose VC-credit counter and line slot counter.

In the same field of endeavor, Chen clearly shows maintaining further comprises:

initializing said VC-credit counter (column 14, lines 63-67 (l.sub.i)) and a line slot credit counter (column 14, lines 40-47(c.sub.i 1)) associated with said fourth virtual circuit to zero (fig. 6 (225 and 227); column 14, lines 40-41 (c.sub.i is set to zero); column 14, lines 63-67 (set l.sub.i to zero));

incrementing said line slot credit counter by a token value (column 0014, lines 52-55) in each cell slot of said communication path, wherein said token value is determined by a length of duration (column 0014, lines 52-55 (incremented once every 1/100 sec)) of cell slots on said communication path;

incrementing said VC-credit counter by one (column 15, lines 45-56 (l.sub.i is incremented)) if said VC-credit counter is already not equal to said maximum number (column 15, lines 45-49 (l.sub.i_m));

decrementing said line slot credit count (column 13, lines 55-57 (decrement c.sub.i) when said VC-credit counter is incremented (Inter-cell gap indicates how many cell slots should elapse between successive transmissions. During the inter-cell gap, bandwidth is used so the slot credit count is decremented. However, VC-credit counter is incremented because the cells are backlogged during inter-cell gap.)); and

decrementing said VC-credit counter by one when a cell related to said fourth virtual circuit is scheduled for transmission (fig. 5 (200), column 13, lines 55-57 (decrement backlog)).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to demonstrate sharing a line bandwidth, as taught by Wei, and

incorporate VC-credit counter and line-slot counter, as taught by Chen, so that data can be handled smoothly.

However, Wei, as modified by Radhakrishnan and Chen, does not specifically disclose inter-cell gap.

In the same field of endeavor, Turner clearly shows the inter-cell gap (column 2, lines 6-12 (inter-cell spacing (Line slot credit must be greater than or equal to the inter-cell gap or it can not transmit. During the gap, there is no data.))).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to demonstrate sharing a line bandwidth, as taught by Wei, and incorporate VC-credit counter and line slot counter, as taught by Chen, and show inter-cell gap, as taught by Turner, so that virtual circuits can be managed efficiently.

Consider **claim 8**, and **as applied to claim 7 above**,

claim 19, and **as applied to claim 18 above**,

claim 30, and **as applied to claim 29 above**,

claim 41, and **as applied to claim 40 above**,

Wei, as modified by Radhakrishnan, Chen and Turner, clearly discloses and shows a method as described.

However, Wei, as modified by Radhakrishnan, Chen and Turner, does not specifically disclose peak maximum slot credit.

In the same field of endeavor, Chen clearly shows a method, further comprising:

computing a peak maximum slot credit (column 2, lines 44-48 (peak rate allocation)) associated with a fifth virtual circuit, wherein said peak maximum slot credit are computed according to a corresponding peak cell rate (PCR) (column 2, lines 44-48 (peak rate allocation));

initializing a peak slot credit associated with said fifth virtual circuit to zero ((column 14, lines 63-67 (I.sub.i)));

incrementing said peak slot credit by said token value (column 0014, lines 52-55) in each cell slot, but said peak slot credit being capped at said peak maximum slot credit (column 14, lines 40-47 (c.sub.i_m1);

decrementing said peak slot credit if a cell associated with said fifth virtual circuit is scheduled for transmission (fig. 5 (200), column 13, lines 55-57);

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to demonstrate sharing a line bandwidth, as taught by Wei, and incorporate peak maximum slot credit, as taught by Chen, so that data can be handled smoothly.

However, Wei, as modified by Radhakrishnan, Chen and Turner, does not specifically disclose inter-cell gap.

In the same field of endeavor, Turner clearly shows the peak inter-cell delay (column 2, lines 6-12 (inter-cell spacing d.sub.i (Line slot credit must be greater than or equal to the inter-cell gap, otherwise it can not transmit. During the gap, there is no data but the bandwidth is still used.))).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to demonstrate sharing a line bandwidth, as taught by Wei, and incorporate peak maximum slot credit, as taught by Chen, and show inter-cell gap, as taught by Turner, so that virtual circuits can be managed efficiently.

Consider **claim 9**, and **as applied to claim 8 above**,

claim 20, and **as applied to claim 19 above**,

claim 31, and **as applied to claim 30 above**,

claim 42, and **as applied to claim 41 above**,

Wei, as modified by Radhakrishnan, Chen and Turner, clearly discloses and shows a method, wherein said fourth virtual circuit is of CBR VC-type, and wherein said maximum number equals 1 (fig. 4 (404,408), column 10, lines 44-52 (If it is CBR, no credit is involved. This is the same as setting the maximum number to 1 to avoid credit processing as in the claim.)).

With respect to **claim 45**, and **as applied to claim 41 above**, it is rejected for the same reason as set forth in **claim 3**.

Claims 10, 21, 32 and **43** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wei (U.S. Patent # 6560196),** in view of **Radhakrishnan et al. (U.S. Patent # 6049526), Chen (U.S. Patent # 5533009),** and **Turner (U.S. Patent Publication #5179556),** and further in view of **Ukon (U.S. Patent Publication #20010008529).**

Consider **claim 10**, and **as applied to claim 8 above**,

claim 21, and **as applied to claim 19 above**,

claim 32, and **as applied to claim 30 above**,

claim 43, and **as applied to claim 41 above**,

Wei, as modified by Radhakrishnan, Chen and Turner, clearly discloses and shows a method, wherein said fourth virtual circuit is the same as said fifth virtual circuit and is of VBR VC-type (fig. 4 (404, 406)), and wherein said maximum number is computed according to a equation, wherein - and x respectively represent a subtraction and a multiplication operation, PCR represents peak cell rate (column 2, lines 20-22 (PCR)), SCR represents sustained cell rate (column 2, lines 20-22 (SCR)), and MBS represents maximum burst size of said fourth virtual circuit (column 2, lines 20-22 (MBC)).

However, Wei, as modified by Radhakrishnan, Chen and Turner, does not specifically disclose the equation for said maximum number.

In the same field of endeavor, Ukon clearly shows the equation for the said maximum number (paragraph 0058 (MBS as defined in TM 4.0)).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to demonstrate sharing a line bandwidth, as taught by Wei, and incorporate the equation for the maximum number, as taught by Ukon, so that virtual circuits can be managed efficiently.

Claims 11, 22, 33 and **44** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Wei (U.S. Patent # 6560196),** in view of **Radhakrishnan et al. (U.S. Patent # 6049526), Chen (U.S. Patent # 5533009),** and **Turner (U.S. Patent Publication #5179556)** and further in view of **Kalkunte et al. (U.S. Patent Publication #20030231635).**

Consider **claim 11**, and **as applied to claim 8 above**,

claim 22, and **as applied to claim 19 above**,

claim 33, and **as applied to claim 30 above**,

claim 44, and **as applied to claim 41 above**,

Wei, as modified by Radhakrishnan, Chan and Turner, clearly discloses and shows the method as described.

However, Wei does not specifically disclose ATM device comprises one of a CPE, a DSLAM, an ATM switch and a edge router.

In the same field of endeavor, Kalkunte et al. clearly show ATM device comprises one of a CPE (paragraph 0027 (CPE)), a DSLAM (paragraph 0027

(DSLAM)), an ATM switch (paragraph 0027 (ATM)) and an edge router (paragraph 0027 (router)).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of invention to demonstrate sharing a line bandwidth, as taught by Wei, and incorporate CPE, DSLAM, ATM and router, as taught by Kalkunte, so that that virtual circuits can be managed efficiently.

Conclusion

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the

Examiner should be directed to Sai-Ming Chan whose telephone number is (571) 270-1769. The Examiner can normally be reached on Monday-Thursday from 6:30am to 5:00pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 571-272-4100.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-2600.

Sai-Ming Chan
S.C./ sc

Sai-Ming Chan

February 24, 2008

Seema S. Rao 2/28/08
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